

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**In re Application of:**

Teck Kheng Lee

**Serial No.:** Not Yet Assigned

**Filed:** March 12, 2004

**For:** INNOVATIVE SOLDER BALL PAD  
STRUCTURE TO EASE DESIGN RULE,  
METHODS OF FABRICATING SAME  
AND SUBSTRATES, ELECTRONIC  
DEVICE ASSEMBLIES AND SYSTEMS  
EMPLOYING SAME

**Confirmation No.:** Unknown

**Examiner:** Unknown

**Group Art Unit:** Unknown

**Attorney Docket No.:** 2269-5351.1US  
(02-0239.01/US)

**NOTICE OF EXPRESS MAILING**

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Date of Deposit with USPS: March 12, 2004

Person making Deposit: Christopher Haughton

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

The present application is a continuation of application Serial No. 10/230,962, filed August 29, 2002, pending.

Pursuant to M.P.E.P. 2001.06(b), the Examiner is respectfully requested to consider the information of record in the prior application, and to confirm in the first Office Action on the merits that such art has in fact been reviewed. A PTO-1449 form listing all of the information of record in the prior application is enclosed herewith.

**Attorney Docket No.: 2269-5351.1US**

This Information Disclosure Statement is filed within three (3) months of the filing date of the above-identified application, and no certification pursuant to 37 C.F.R. § 1.97(c) or a fee pursuant to 37 C.F.R. 1.17(p) is required.

Respectfully submitted,



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Date: March 12, 2004  
TNB/ps:ljb

Enclosures: Form PTO-1449

Document in ProLaw

<b>Form PTO-1449</b>  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <i>(Use several sheets if necessary)</i>	<b>Docket Number (Optional)</b> <b>2269-5351.1US</b> <b>(02/0239.01/US)</b>	<b>Application Number</b> <b>Not Yet Assigned</b>
	<b>Applicant</b> <b>Teck Kheng Lee</b>	
	<b>Filing Date</b> <b>March 12, 2004</b>	<b>Group Art Unit</b> <b>Unknown</b>

### U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	3,392,442	07/1968	Napier et al.			
	5,767,010	06/1998	Mis et al.			
	5,773,359	06/1998	Mitchell et al.			
	5,872,399	02/1999	Lee			
	6,107,180	08/2000	Munroe et al.			
	6,111,321	08/2000	Agarwala			
	6,201,305 B1	03/2001	Darveaux et al.			
	6,249,044 B1	06/2001	Kao et al.			
	6,316,828 B1	11/2001	Tao et al.			
	6,399,417 B1	06/2002	Lee et al.			
	6,404,064 B1	06/2002	Tsai et al.			

### FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

### OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

		http://www.maxim-ic.com/1st_pages/UCSP.htm, "Wafer-Level Chip-Scale Package," Dallas Semiconductor, date unknown, 10 pages.
		"CSP Present and Future," date unknown, 3 pages.
		TARTER et al., "Ball Grid Array Performance Characteristics; A User's Design Guide," File Creation Date: March 31, 1999.

<b>EXAMINER</b>	<b>DATE CONSIDERED</b>
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**EXAMINER:** Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

<b>Form PTO-1449</b>  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <i>(Use several sheets if necessary)</i>				Docket Number (Optional) <b>2269-5351.1US (02/0239.01/US)</b>		Application Number <b>Not Yet Assigned</b>	
				Applicant <b>Teck Kheng Lee</b>			
				Filing Date <b>March 12, 2004</b>		Group Art Unit <b>Unknown</b>	

  

U.S. PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

  

FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

  

OTHER DOCUMENTS		(Including Author, Title, Date, Pertinent Pages, Etc.)
		"BGA (Ball Grid Array)," National Semiconductor Corporation, September 1999, pp. 1-7, Application Note 1126.
		MicroStar BGA Packaging Reference Guide, September 1999, 15 pages, Literature Number: SSYZ015B.
		"Mounting Technology," Sharp, File Creation Date: October 10, 2000, pp. 12-36.
		"Chapter 7: Board Design and Layout Considerations," FBGA User's Guide, April 12, 2002, pp. 41-45, Version 4.1.

  

EXAMINER	DATE CONSIDERED
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